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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/854,813	05/14/2001	Eric H. Johnson	17732-3675000	8846
7590	02/03/2004		EXAMINER	
Edwin H. Paul Cesari and McKeanna, LLP 88 Black Falcon Avenue Boston, MA 02210			SAGAR, KRIPA	
			ART UNIT	PAPER NUMBER
			1756	

DATE MAILED: 02/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/854,813

Applicant(s)

JOHNSON ET AL. 

Examiner

Kripa Sagar

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 November 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 January 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed 11/6/03 has been entered. Claims 1-5,18,24 have been amended; no new matter has been added. Claims 1-24 are under consideration.

Claim Rejections - 35 USC § 112

2. The amendment overcomes the rejections under 35USC112 presented in the earlier office action.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koh in view of US Pat. 5481475 to Young .

Koh teaches *planarization* of structures *with large step-heights* ("severe non-flat topologies" recited in independent claims 1,10 and elsewhere). The *equipment* DOF (depth-of-focus) is considered as recited in claims 1,2,11. The *layout is changed* [claimed in 1,2,10] to facilitate planarization (Fig.2). This is rudimentary prior-art (col.1;line.46-col.2;line.15). In Koh's invention (Fig.3-7) a global planarization pattern (46) is formed ("layout change") on a semiconductor substrate with a high step-height integrated circuit structure. The initial structure (Fig.3) is formed by etching the

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semiconductor as recited in claims 3,12 (col.6;line:42-54). A planarizing dielectric layer (50) is deposited on the structure. The dielectric layer is reflowed to planarize the structure that *substantially fills* the non-flat topologies as listed in claim 10,15 (col.3;line.1-13). A *blanket photoresist* is coated to a *thickness* such that it is within the DOF of the lithographic tool [Claim 2,11] (col.3;line. 33-37). Several *conformal layers* (36,40,44) are coated over the structures as required in claims 4,5,13,14. The conformal layers may include a layer (36) of insulator [cl.7,16] that is *blanket deposited* [cl.8,17](col.6;line.33-41). One of the conformal layers may be a *polysilicon* (42) layer[cl.6,15] (col.7;line.13-17). Thus Koh teaches most of the elements of claims 1-17.

Koh teaches adjusting the layout dimensions and discusses the process variables. It does not *explicitly* correlate the adjustments to the variables as required in claims 1,10.

Photolithography is a demanding art wherein all factors are considered and modeled before implementing a process (Young: col.1;line.13-24). Young teaches the steps of modeling the process and modifying the layout and process parameters (Fig.8). The process parameters are correlated with the layout dimensions in a feedback loop (col.6;line.63-67).

One of ordinary skill in the art at the time the invention was made would be motivated to evaluate Koh's process variables and integrate them into a process model as taught by Young; because Young teaches that this identifies problems early in the process and leads to more robust designs (col.6;line.58-64).

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5. Claims 18-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koh in view of Young and further in view of US Pat. 5963788 to Barron et al. and further in view of US Pat. 5919548 to Barron et al. (Barron2) and further in view of US Pat. 6103399 to Smela et al..

The teachings of Koh have been discussed above. It does not teach MEMS devices or medical implements recited in claims 18-24.

Young does not teach fabricating MEMS devices or micro-medical implements recited in claims 18-24.

Barron teaches that MEMS structures have severe non-flat topologies (col.1;line.53-63) and integrating such devices with semiconductor circuits pose special challenges to fabrication (col.2;line.24-27). The process of forming an integrated device is shown in Figs.2-13. After the fabrication of MEMS devices in a cavity, the cavity is filled with a conformal oxide (32) layer(Fig.5, col.7;line.33-37). The oxide layer is partially covered and etched back followed by a polishing step.(col.7;line.40-49). The planarized surface is amenable to fabrication of electronic circuitry using conventional steps, as shown by Koh. Barron teaches that this technique can be used to fabricate a variety of devices such as motors, pressure [cl.21] /flow / chemical [cl.22] sensors, accelerometers [cl.23] and the like (col.4; line.35-49).

Barron does not specifically teach the fabrication of a mirror [cl.19], pump[cl.20] or micro-medical implements [cl.24].

Barron2 teaches methods of planarizing MEMS structures prior to further processing. This might be imperative in forming mirrors [cl.19] (col. 3; lines.45-50).

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Barron2's invention is similar to that of Barron and includes integration of MEMS structures with electronic circuitry.

Barron2 does not teach pumps or micro-medical implements.

Such sensors are widely known in prior art as shown by Smela (col.1;line.30-53).

Peristaltic pumps may be integrated into medical devices as recited in cl.20, 24.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form diverse sensors using the teachings of Smela ,Barron2 and Barron and using the planarizing steps of Koh, Young,Barron2 and Barron because Barron and Barron2 teach that this facilitates the integration of the sensor(device) with the electronic circuitry and Smela teaches that these devices are widely known and successfully fabricated.

Response to Arguments

6. Applicant's arguments filed 11/6/03 have been fully considered but they are not persuasive.

Applicant has argued that Olsen does not teach adjusting the layout dimensions as result of evaluating the process variables. Examiner agrees that Olsen teaches the methods of planarization and the *reasons* for planarizing. Not all of the factors are included in the reasons.

Applicant argues that Koh similarly teaches planarization but does not evaluate the equipment and process variables. It is argued that Koh does not change the layout dimensions in response to process variables. As shown above with specific citations, Koh teaches resist thickness adjustment considering the DOF of the equipment and

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layout adjustment based on the photoresist and underlayers. This is standard practice in the art as shown by Young.

The instant invention is a generic outline of process steps, routinely used in qualifying a process. Numerous references may *be readily obtained* to confirm this. US Pat. 6355387 to Fujinaga (not used in the rejection) teaches the steps of the process used for adjusting the layout dimensions on a variable topology. The claims are non-specific and contain no novel or unobvious elements.

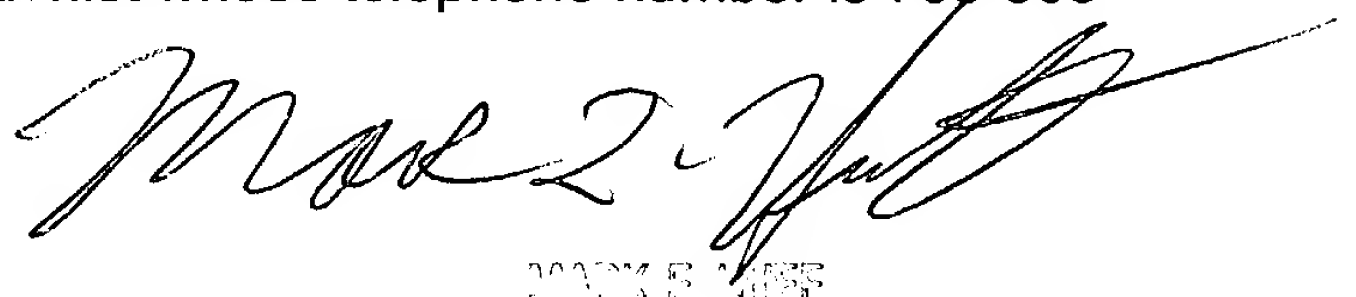
Conclusion

7. The art made of record and not relied upon is considered pertinent to applicant's disclosure. US PG PUB 2003/0237064 to White et al. teaches all the elements of the instant claims. White is not prior art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kripa Sagar whose telephone number is 571-272-1392. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark F Huff can be reached on 571-272-1385. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0661.



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MH/ks